L Number	Hits	Search Text	DB	Time stamp
1	3632	716/$.ccls.	USPAT	2003/02/04 13:51
2	500	((716/12) or (716/13) or (716/14)).CCLS.	USPAT	2003/02/04 13:54
3	10	(((716/12) or (716/13) or (716/14)).CCLS.) and linear near3 (program$4 or problem)	USPAT	2003/02/04 14:02
4	9765	net and partition$3 snf rout$3 and linear near2 program$4 and edge	USPAT	2003/02/04 14:05
5	461	716/$.ccls. and (net and partition$3 snf rout$3 and linear near2 program$4 and edge)	USPAT	2003/02/04 14:05
6	92	(((716/12) or (716/13) or (716/14)).CCLS.) and (net and partition$3 snf rout$3 and linear near2 program$4 and edge)	USPAT	2003/02/04 14:05
7	90	((((716/12) or (716/13) or (716/14)).CCLS.) and (net and partition$3 snf rout$3 and linear near2 program$4 and edge)) not ((((716/12) or (716/13) or (716/14)).CCLS.) and linear near3 (program$4 or problem))	USPAT	2003/02/04 14:41
8	326	(716/12).CCLS.	USPAT	2003/02/04 14:41
9	2	((716/12).CCLS.) and (partition$3 with region)	USPAT	2003/02/04 14:42
10	4	((716/12).CCLS.) and (linear near3 (program$3 or problem))	USPAT	2003/02/04 14:44
11	2	partition$3 same net same edge same rout$3	USPAT	2003/02/04 14:47

SEARCH RESULTS [PDF Full-Text (364 KB)] PREVIOUS DOWNLOAD CITATION

Four-bend top-down global routing

Cho, J.D. Sarrafzadeh, M.
Sch. of Electr. & Comput. Eng., Sungkyunkwan Univ., Suwon;

This paper appears in: **Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on**
On page(s): 793-802
Volume: 17, Sep 1998
ISSN: 0278-0070
References Cited: 31
CODEN: ITCSDI
INSPEC Accession Number: 6041727

Abstract:
We propose a new global net distribution approach for high-performance m×m two-dimensional arrays of very large scale integration and multichip-modules. objective is to route n nets with minimum density of global cells, using a “small” number of bends. There are a number of applications wh is necessary to limit the number of bends on each wire. For example, it is desir to limit the number of bends on each microstrip (transmission) line, for misma of line impedance can cause reflections from the junction points such as bends vias. Furthermore, for high-performance routing, intersections of wires cause t use of more vias, which in turn require the use of more routing resources (bec of the larger via pitch). This is the first paper that addresses a graph-theoretic framework to solve the bend-constrained global routing problem in two-dimen arrays. In this paper, at each level of an underlying quad-tree, we present a n four-bend routing algorithm by decomposing the original problem at level i int subproblems that can be solved exactly based on a two-stage approach of smaller-sized linear program followed by min-cost flow networks. The overall (entire level of the four-way partition hierarchy) constraint and variable size for first stage is $O(md_o)$, while the overall run time for the second stage is $O(n^3 lo n^2)$. The time complexity of such a hierarchical approach is one order of magni less than one of constructing a global routing using the min-cost-flow-based fl design approach. Last, we present an extension that permits a limited degree control over the number of bends. The proposed algorithm can also be used fo estimating the wireability in the early design planning stage for high-level synthesis. Experimental results showed the effectiveness of the proposed algor

Index Terms:
VLSI circuit layout CAD computational complexity flow graphs high level synthesis integrated circuit layout linear programming logic partitioning network routing wiring

Documents that cite this d cument

Your search matched **2** of **916175** documents.

A maximum of **2** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text
Then click **Search Again**.

wiring <and> problem <and> linear <and> subproblem

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Linear complexity algorithms for hierarchical routing**
Hachtel, G.D.; Morrison, C.R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions o
Volume: 8 Issue: 1 , Jan 1989
Page(s): 64 -80

[Abstract] [PDF Full-Text (1500 KB)] **IEEE JRN**

2 **Four-bend top-down global routing**
Cho, J.D.; Sarrafzadeh, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions o
Volume: 17 Issue: 9 , Sep 1998
Page(s): 793 -802

[Abstract] [PDF Full-Text (364 KB)] **IEEE JRN**

Your search matched **16** of **916175** documents.

A maximum of **16** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text
Then click **Search Again**.

linear <and> problem <and> route <and> net

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Cell height reduction by routing over-the-cells**
How-Rern Lin; Hourng-Wern Perng; Yu-Chin Hsu;
Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on , Volume: 5 , 10-13 May 1992
Page(s): 2244 -2247 vol.5

[Abstract] [PDF Full-Text (348 KB)] **IEEE CNF**

2 **An efficient algorithm for the net matching problem**
Carragher, R.J.; Cheng, C.-K.; Fujita, M.;
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical Papers., 1993 IEE International Conference on , 7-11 Nov 1993
Page(s): 640 -644

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

3 **A new global router based on a flow model and linear assignment**
Meixner, G.; Lauther, U.;
Computer-Aided Design, 1990. ICCAD-90. Digest of Technical Papers., 1990 IEE International Conference on , 11-15 Nov 1990
Page(s): 44 -47

[Abstract] [PDF Full-Text (372 KB)] **IEEE CNF**

4 **Hybrid leader-follower and fuzzy-Petri-net traffic rate control and supervisi n in network systems**
Dimirovski, G.M.; Yuanwei Jing; Siying Zhang;
Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2001.